Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VEE**
2. **VCC**
3. **C4**
4. **C3**
5. **C2**
6. **C1**
7. **V opt**
8. **GND**
9. **A1**
10. **B1**
11. **A2**
12. **B2**
13. **A3**
14. **B3**
15. **A4**
16. **B4**

**DIE ID**

**8 7 6 5 4 3 2**

**10 11 12 13 14 15**

**9**

**1**

**16**

**MX987**

**.049”**

**.067”**

**GRADE 1 (No circuitry in streets)**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .003”**

**Mask Ref: MX987**

**APPROVED BY: DK DIE SIZE .049” X .067” DATE: 7/19/17**

**MFG: IXYS THICKNESS .0010” P/N: MADRMA0001 / FV00073**

**DG 10.1.2**

#### Rev B, 7/19/02